60 GHZ GaAs MMIC TECHNOLOGY FOR A HIGH DATA RATE MOBILE BROADBAND DEMONSTRATOR

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Abstract

A millimeter-wave front end demonstrator for broadband pico-cell networks has been developed using 60 GHz GaAs MMIC technology. The following sub-assemblies are integrated in the demonstrator: a 56.8 GHz phase locked LO, an upconverter from 5.2 - 6.2 GHz IF to a 62 - 63 GHz band, a double-channel low noise downconverter from the 62 - 63 GHz band to an IF of 5.2 - 6.2 GHz, and a power amplifier for the 62 GHz to 66 GHz band. For a duplex operation a second upconverter module operating at 65 - 66 GHz (IF 8.2 - 9.2 GHz) is used. All monolithic HFET and PHFET circuits are realised using subquarter micron technologies. For the fully assembled receivers overall noise figures of less than 10 dB have been measured. Field tests have proven the ability to transmit data nearly error free over a distance of 200m.

Introduction

Many applications in wireless communications will, in the future, require mobile broadband systems providing high data rate radio links. Examples are multimedia offices, telerobotics, high definition digital cameras, or computer interconnections. Within the European research project Mobile Broadband System (MBS; a part of the RACE program) a demonstrator has been realized which is able to transmit more than 34 Mbit/s in a mobile environment. Because of the high bandwidth requirement a frequency range of 62 to 63 GHz and 65 to 66 GHz has been selected. A widely spread MBS system needs a low cost, low volume and small size high quality millimeter wave technology which can easily be inserted into large volume production programs. Hence, for the demonstrator millimeter wave GaAs IC's have been developed using subquarter micron transistor technologies. The realized millimeter wave front end consists of four subassemblies implemented in a single housing: a 56.8 GHz phase locked oscillator, an upconverter from C-band to 65 - 66 GHz, a double channel low noise downconverter from 62 - 63 GHz to C-band, and a V-band power amplifier. Performances of these building blocks as well as integration technologies have partly been published earlier [1-4]. In this paper MMIC and subassembly developments as well as demonstrator measurement results are summarized.

Front end architecture

In Fig. 1 a functional block diagram of the millimeter wave integrated front end is shown. The 56.8 GHz LO uses three MMIC devices:

- a DRO (28.4 GHz) and power splitter chip
- a multifunction chip containing doubler, filter, power splitter and LO amplifiers
- an analog divider chip

The downconverter assembly is composed of five MMICs:

- two five stage LNAs
- two mixers with integrated pre-amplifiers
- an LO buffer amplifier with power splitter

The upconverter contains four MMICs:

- a commercial IF amplifier
- a two-stage LO buffer amplifier
- a SSB upconverter mixer
- a four-stage RF amplifier

The complete transceiver consisting of millimeter wave head, a second LO stage and an IF baseband processing unit [5] is designed for full duplex operation using separate antennas for transmit and receive mode.

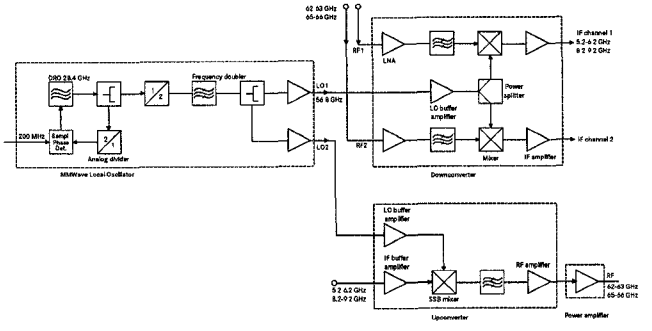

Fig. 1: Block diagram of the millimeter wave front end

Upconverter

The single side-band upconverter mixer is a balanced configuration using Lange couplers for splitting LO signal and combining RF signal. A bandstop filter is integrated for reflecting the unwanted lower side-band. The mixing Schottky diode is realized in an MESFET compatible burried layer technology. Typical conversion loss in the 62 GHz to 66 GHz band is 6 dB, typical noise figure is 6.5 dB. LO buffer and RF amplifiers are fabricated using 0.18 µm gate length PHFET technology. For the LO amplifier single-stub input and output matching circuits are used. Unconditional stability is obtained by means of a thin film resistor and MIM capacitor

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parallel configuration in each transistor drain circuit. Fig. 2 shows the realized chip with a size of 2.85 mm x 1.7 mm.

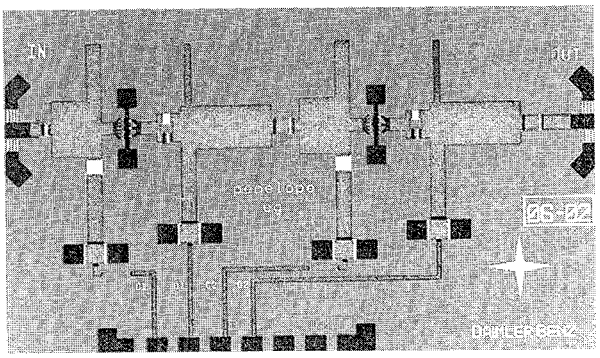

Fig. 2: Photograph of the upconverter LO buffer

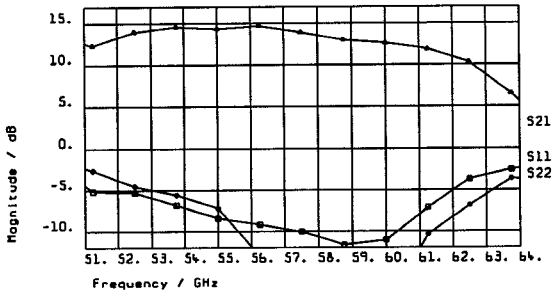

Fig. 3: Measured S-parameters of the LO buffer amplifier

Measured small-signal S-parameters of the two-stage device are plotted in Fig. 3 demonstrating a gain of about 14 dB at 56.8 GHz. Input matching and interstage circuitry for the four-stage RF amplifiers are performed by side-coupled microstrip sections. Parallel configurations of resistors and capacitances in the drain circuits yield high attenuations at low frequencies and quench spurious oscillations.

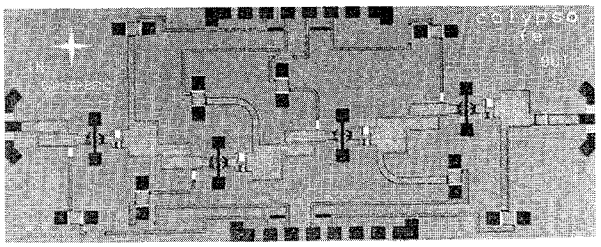

Fig. 4: Photograph of the RF amplifier

The amplifier chip for the 65 GHz channel as shown in Fig. 4 has a size of 3.4 mm x 1.8 mm. Measurement results are demonstrated in Fig. 5. At 65 GHz a gain of more than 20 dB with an associated noise figure of 4 dB are obtained. The upconverter module is assembled using a commercial IF amplifier and a side-coupled bandpass filter (see Fig. 1) realized on alumina substrate. Fig. 6 shows output power and conversion gain of the 65 GHz channel plotted versus IF frequency. A gain of more than 9 dB is achieved, the output power is between + 14 dBm and + 15 dBm.

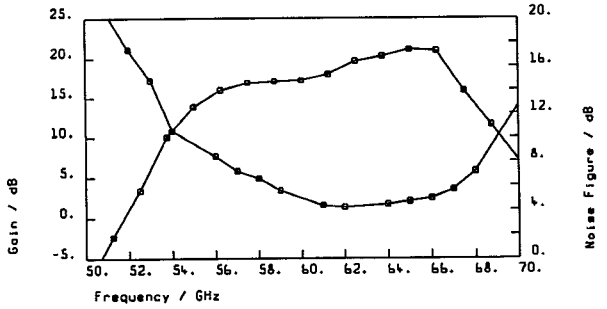

Fig. 5: Gain and noise figure of the RF amplifier

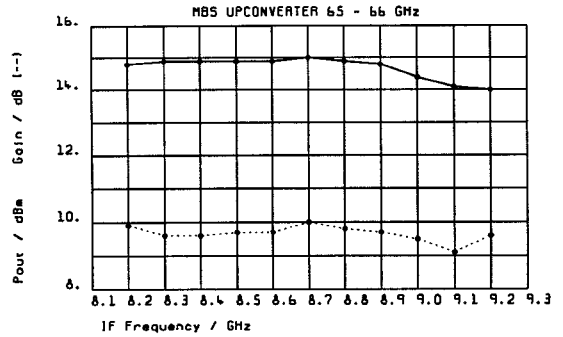

Fig. 6: Output power and gain of the integrated upconverter module

Power amplifier

For the power amplifier a three-stage double-balanced design approach has been selected. Lange couplers are used at the input and output to combine the two parallel chains. The amplifier (see Fig. 7, chip size 3 mm x 4 mm) is realized using 0.15 µm PHFET devices with 60 µm gate width in the second and third stages. The output power of the amplifier as a function of frequency at two different input power levels is plotted in Fig. 8. About 17.5 dBm is obtained at 64 GHz and more the 17 dBm over the entire 62 GHz - 66 GHz frequency range.

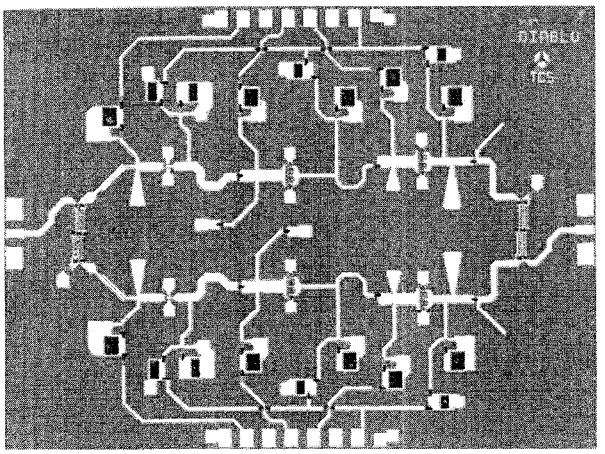

Fig. 7: Photograph of the power amplifier

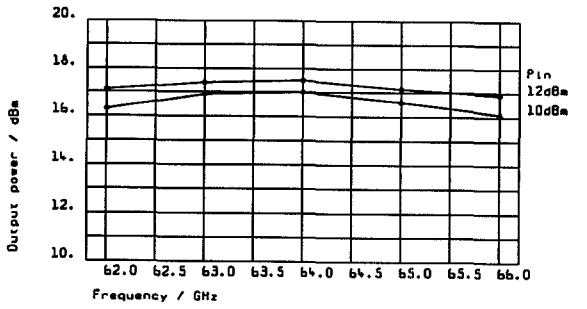

Fig. 8: Measured power amplifier output performance vs input power

Local oscillator 56.8 GHz (MPLO)

The MPLO architecture is given in Fig. 1. A harmonic generation has been chosen for the millimetre-wave oscillator. The following five functions have been developed using MMIC technology:

- a Voltage Controlled Dielectric Resonator Oscillator (VCDRO) at 28.4 GHz
- a frequency doubler from 28.4 to 56.8 GHz
- a buffer amplifier/power divider at 56.8 GHz
- an analogue frequency divider from 28.4 to 14.2 GHz
- a bandpass filter.

The VCDRO is based on a 2 x 50µm HFET active device with a series feedback (Fig. 9, chip size 2 mm x 1.5 mm).

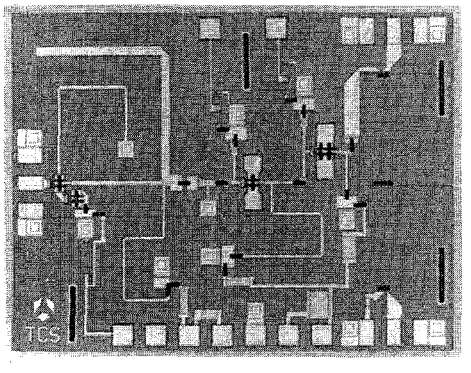

Fig. 9: Photograph of the 28.4 GHz VCDRO chip

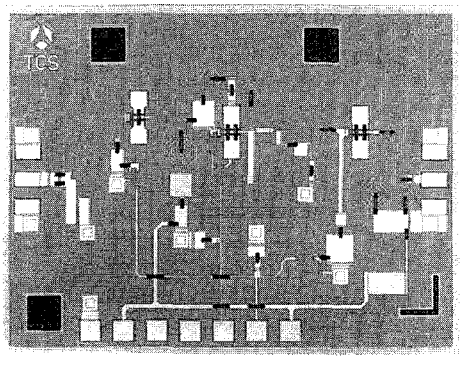

Fig. 10: Frequency divider chip

An essential part of this oscillator is the dielectric resonator on an adjacent alumina substrate coupled to a microstrip line. The voltage controlled tuning is achieved by a "cold HFET" (biased at Vds=0V) used as a varactor. A buffer amplifier provides two outputs, one for the doubler and one for the divider. The dynamic frequency divider uses the regenerative properties of a non linear device coupled to a feedback loop. Measurements exhibit a bandwidth greater than 12% and a conversion gain greater than 8 dB (0 dBm input power). The divider chip (2 mm x 1 mm) is shown in Fig. 10. A single ended structure has been chosen for the frequency doubler. It consists of a 28.4 GHz input amplifier, a second stage with a HFET biased near pinch-off for optimum second harmonic generation, and an output 56.8 GHz amplifier third stage. A conversion gain of 5 dB at an output power of 5 dBm is achieved. The output buffer amplifier is based on a Lange coupler followed by three-stage amplifiers on each branch. Output power is greater 6 dBm, gain higher 10 dBm. The filter is a side-coupled bandpass configuration. Doubler, filter, and two LO amplifiers as well as a power splitter are integrated on a multifunction GaAs chip shown in Fig. 11. The chip size is 2 mm x 4.5 mm. Phase noise measurement of the entire MPLO module yield values better - 100 dBc/Hz at 1 MHz and - 70 dBc/Hz at 10 kHz offset. Output power signals at 56.8 GHz are about 8 dBm at 0°C decreasing to 6.7 dBm at 50°C.

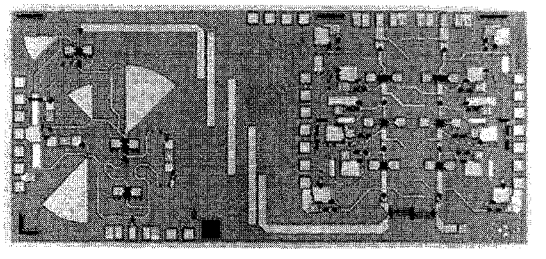

Fig. 11: MPLO multifunction chip

Downconverter

The receivers exhibit dual channel capability (see Fig. 1) in order to cope with the strong fading environment at 60 GHz, and are composed of five MMICs. Each channel comprises a 5-stage low noise millimeter wave amplifier (Fig. 12, chip size 1.2 mm x 2.85 mm) and a multifunction chip integrating a 4-stage low noise amplifier and a mixer.

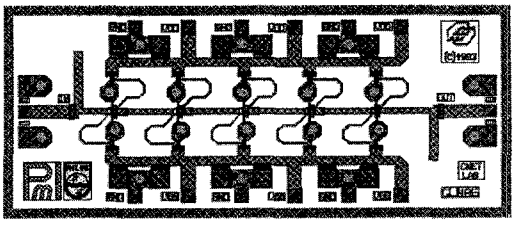

Fig. 12: Chip layout of the downconverter 5-stage LNA

In addition to these, a power splitter provides the 56.8 GHz LO signals to the mixers. To reject the image frequency, thin film edge coupled line filters were chosen (see Fig. 13). The design of the low

noise stages implements 4 x 15µm transistors biased at 60% Id_{ss}. Interstage matching networks use a simple capacitor-transmission line series configuration. The mixers have a single FET drain-pumped structure. A noise figure of 7.5 dB ± 0.5 dB with associated gain of 19.5 dB ± 1.5 dB are obtained over the 62 - 63 GHz RF band (Fig. 14) taking into account the losses of two waveguide to microstrip transitions (0.7 dB each).

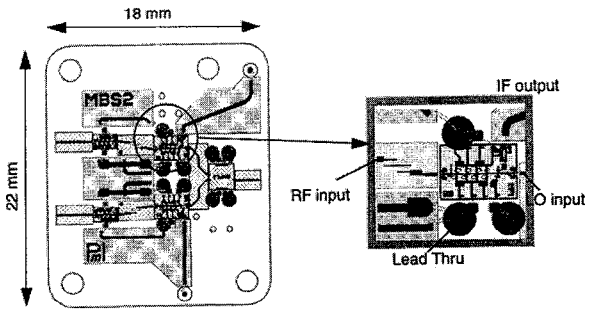

Fig. 13: Top view of the downconverter submodule and expanded view of the LNA mixer chip (2.0 mm x 2.85 mm)

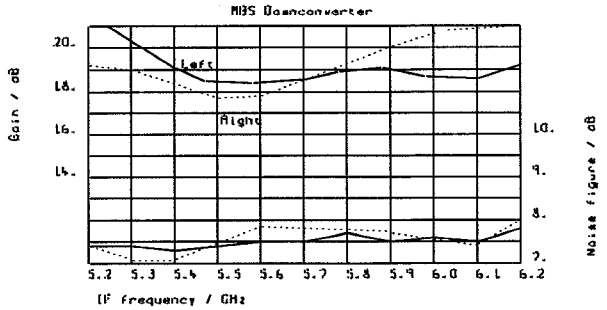

Fig. 14: Gain and noise figure for the two channels of the low-noise downconverter submodule

Demonstrator results

The millimeter-wave subassemblies described here are used in the full duplex mm-wave heads for the MBS Demonstrator. In the transmit part a 160 MHz IF signal modulated with 32 Mbit/s is upconverted to a carrier in the 62 GHz to 63 GHz range. In the mobile station an output power of 19 dBm is obtained using a Gunn injection locked oscillator as output stage. The base station transmitter uses the integrated front end and achieves an output power of approximately 15 dBm. Both base- and mobile station receivers have two channels for diversity reception. The millimeter-wave signal is downconverted via several intermediate frequency stages to a low IF, dynamically compressed, and supplied to the demodulator. For the base- and mobile station receivers overall noise figures of less than 10 dB have been measured. Field test trials using the mm-wave transceivers prove the ability to transmit data or digitized video image nearly error free over 200 m distance.

Conclusion

A set of monolithically integrated GaAs chips for the 60 GHz range has been realized for mobile broadband communications. The MMICs used for oscillator, upconverter, and downconverter functions mainly are realized using sub-quarter micron gate length HFET and PHFET processes of three European foundries. MBS demonstrator measurement results show on the one hand the feasibility and maturity of these technologies and on the other hand the performances of a wireless communication system operating in the millimeter wave range.

Acknowledgement

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